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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,006	03/03/2004	Chung-Hui Chen	TSMC2003-0803(N1280-00040	4259

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DUANE MORRIS LLP
IP DEPARTMENT (TSMC)
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103-4196

EXAMINER

COX, CASSANDRA F

ART UNIT PAPER NUMBER

2816

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/792,006

Applicant(s)

CHEN, CHUNG-HUI

Examiner

Cassandra Cox

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-8,10-13,15-19 and 21-24 is/are rejected.
- 7) ☒ Claim(s) 3,9,14 and 20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments filed 05/25/06 have been fully considered but they are not persuasive. The rejection is repeated below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 4-8, 10-13, 15-17, and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami (U.S. Patent No. 4,437,072).

In reference to claim 1, Asami discloses in Figure 2 a clock lock detection circuit comprising: a first input indicating an edge of a first clock (S3); a second input indicating a corresponding edge of a second clock (S4) wherein the second clock is expected to be synchronized with the first clock with an allowable time difference; a difference generation module (11) for generating a difference signal based on the time difference between the first and second inputs; and a voltage divider module (12, 22) having an inverter (12) for receiving the difference signal and generating an indication voltage which varies based on a change of the time difference between the first and second inputs. Asami does not disclose that the inverter is a CMOS inverter. It is well known to one skilled in the art that inverters may be designed using many different processes one of which is CMOS. Therefore, it would have been obvious to one skilled in the art at the time of the invention that the inverter of Asami could be formed using a CMOS process

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(since Asami does not disclose exactly what type of inverter is used) for the advantage of saving power (because CMOS inverters are commonly used as low power alternatives to other inverter types). The same applies to claims 12 and 24.

In reference to claim 2, Asami discloses in Figure 2 wherein the voltage divider module (12, 22) further comprises a capacitor (22) wherein the inverter (12) has first and second supply voltages (which are not shown but are considered to be inherent in all inverters) with the capacitor connected to the second supply voltage (which in this case would be ground) and an output of the CMOS inverter (12). The same applies to claim 13.

In reference to claim 4, Asami discloses in Figure 2 wherein the circuit further comprises a voltage comparator (21) for comparing the indication voltage against a predetermined threshold voltage for generating a lock signal indicating whether the time difference is within the allowable time difference. The same applies to claims 7, 8 and 22-23 (see also the rejection of claim 2 above), 15 and 21.

In reference to claim 5, Asami further discloses in Figure 2 that the voltage comparator (21) is a Schmitt trigger. The same applies to claims 10 and 16.

In reference to claim 6, Asami discloses in figure 4 a buffer module (13) passing the lock signal. The same applies to claims 11 and 17.

4. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami (U.S. Patent No. 4,437,072) in view of Tsinker (U.S. Patent No. 6,323,692)

In reference to claim 18 Asami discloses all the limitations of the phase locked loop comprising a clock lock detection circuit as mentioned above with respect of claim 7. Asami does not disclose the first flip-flop, the second flip-flop, and the reset signal generator. Tsinker discloses in Figure 4 a phase comparator comprising a first flip-flop (150) receiving a first clock (REF. CLOCK) and generating a first signal (UP) indicating an edge of the first clock; a second flip-flop (152) receiving a second clock (FILTER CLOCK) and generating a second signal (DOWN) indicating a corresponding edge of the second clock wherein the edge of the second clock signal is expected to be close to the edge of the first clock signal within an allowable time difference (since the second clock signal is seen to be the adjusted output of the phase lock loop); and a reset signal generator (154, 156, 158) using the first and second signals to generate a reset signal (RST) for the first and second flip-flops. It would have been obvious to one skilled in the art at the time of the invention that the phase comparator of Tsinker could be used to replace the phase comparator of Asami for the advantage of utilizing a phase detector able to compensate for a phase slipping condition (see Tsinker column 4, lines 28-38).

In reference to claim 19, Asami further discloses the voltage divider module (12, 22) has an inverter (12) and a capacitor (22) wherein the inverter (12) has first and second supply voltages (which are not shown but are considered to be inherent in all inverters) with the capacitor connected to the second supply voltage (which in this case would be ground) and an output of the CMOS inverter (12). Asami does not disclose that the inverter is a CMOS inverter. It is well known to one skilled in the art that inverters may be designed using many different processes one of which is CMOS.

Therefore, it would have been obvious to one skilled in the art at the time of the invention that the inverter of Asami could be formed using a CMOS process (since Asami does not disclose exactly what type of inverter is used) for the advantage of saving power (because CMOS inverters are commonly used as low power alternatives to other inverter types).

Allowable Subject Matter

5. Claims 3, 9, 14, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claims 3, 9, 14, and 20 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the difference generation module is an XOR gate (202) in combination with the rest of the limitations of the base claims and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 05/25/06 have been fully considered but they are not persuasive. Applicant argues that the inverter of Asami is not a voltage divider. This argument is not persuasive, since applicant clearly claims an inverter as part of a voltage divider and further defines in dependent claims that the voltage divider also includes a capacitor. The combination of an inverter and a capacitor is clearly shown in the Figure 2. It is this combination of the two that the examiner is relying on to read on the applicants voltage divider. There is no reason for the examiner to believe that the

applicant's combination of an inverter (CMOS) with a capacitor functions as a voltage divider, while the same combination in the prior art reference, Asami, does not. The rejection is maintained and made final.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays 7:30 AM to 4:00 PM.

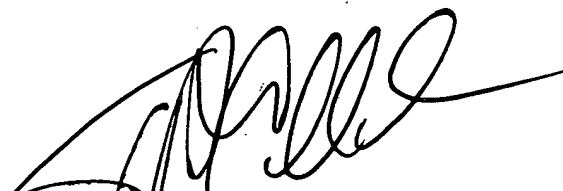
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

Ce

September 3, 2006



TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800